

**REMARKS**

Amendments to claims 1, 11, and 23 are to incorporate limitations from claims 2, 12, and 24, respectively. Amendments to claims 3 and 13 are to change claim dependency. No new matter has been added.

**I. CLAIM REJECTIONS UNDER U.S.C. § 103**

**Pirolli and Moll**

Claims 1-3, 9, 11-13, 19, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,098,064 (Pirolli) in view of U.S. Patent No. 5,600,316 (Moll).

Claims 1, 11, and 23 each recites determining an existence of data redundancies *by calculating row differences between successive rows in prefetch data*. Applicants agree with the Examiner that Pirolli does not disclose or suggest determining redundancy of prefetch data, much less, determining redundancy of prefetch data by calculating row differences. According to the Office Action, column 12, lines 33-56, and figures 8a-8c of Moll allegedly discloses calculating row difference to determine an existence of data redundancy. However, the cited passage actually discloses:

The basis for data compression is to remove the repeated bits because they need not be stored, but rather regenerated at a later time.

FIG. 8a shows five 4-bit characters where the first bit of each character is a one, and the third bit of each character is a zero. This example of the invention removes the 1st and 3rd bits of each character and sends the remaining bits, in this case as 2 bit characters. To designate which bits to remove (and later regenerate), the control data contains a mask which has the 1st and 3rd bits set to one (remove) and the remaining bits reset to zeros (retain). The first 4 bit character of the data involved in repetition is transmitted as the pattern, such as pattern 457 in FIG. 4. The pattern shows the state (1's or 0's) of the repeated bits for later use when regenerating the data.

FIG. 8b shows a similar case using a CVSD coded audio frequency as an example. FIG. 8c shows a similar case using ASCII coded data. FIG.

8d shows the technique of removing the repeated bits before storage or transmission using the data of FIG. 8a. The mask bits are in an end around mask shift register 890 moving at the same clock rate as the shifting in data register 114. The mask register bits cause the data register bits to be either thrown away via AND gate 887 or to be stored or transmitted via AND gate 889.

As such, the cited passage discloses creating a mask to address data redundancy (see figures 8a-8c), but does not disclose or suggest calculating row differences to determine data redundancy. In fact, the cited passage does not even describe how an existence of data redundancy is determined, and describes a masking technique to manage data redundancy (only after an existence of data redundancy is determined). For at least the foregoing reason, claims 1, 11, and 23, and their respective dependent claims, are believed allowable over Pirolli, Moll, and their combination.

Applicants further note that Pirolli, rather than identifying redundancy of prefetch data, specifically teaches addressing insufficient space in local cache by transferring prefetch data that have low probabilities of being requested to a server, while keeping prefetch data that have high probabilities of being requested in a local cache (column 2, line 62 to column 3, line 30). Because Pirolli specifically requires a different technique from that taught in Moll to address the same problem, Pirolli clearly teaches away from Moll, and therefore, cannot be combined with Moll to form the subject matter of claims 1, 11, and 23. For this additional reason, claims 1, 11, and 23, and their respective dependent claims, are believed allowable over Pirolli, Moll, and their combination. Applicants note that this “teach away” argument was presented in the last response, but does not appear to have been addressed by the Examiner.

#### Agarwal and Moll

Claims 1-3, 9, 11-13, 19, and 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,822,749 (Agarwal) in view of Moll. Applicants agree with the Examiner that Agarwal does not disclose or suggest determining redundancy of prefetch data, much less, determining redundancy of prefetch data by calculating row differences. However, as

similarly discussed, Moll also does not disclose or suggest this limitation, and therefore fails to make up the deficiency present in Agarwal. Since both Agarwal and Moll do not disclose or suggest the above limitation, they cannot be combined to form the resulting subject matter of claims 1, 11, and 23. For at least the foregoing reason, claims 1, 11, and 23, and their respective dependent claims, are believed allowable over Agarwal, Moll, and their combination.

Applicants further note that Agarwal specifically teaches addressing insufficient space in local cache by prefetching information having a size that matches a request (column 3, lines 35-40). Because Agarwal requires a different method from that taught in Moll to address the same problem, Agarwal actually teaches away from Moll, and therefore, cannot be combined with Moll to form the subject matter of claims 1, 11, and 23. For this additional reason, claims 1, 11, and 23, and their respective dependent claims, are believed allowable over Agarwal, Moll, and their combination. Again, Applicants note that this “teach away” argument was presented in the last response, but does not appear to have been addressed by the Examiner.


**CONCLUSION**

Based on the foregoing, all remaining claims are believed in condition for allowance. If the Examiner has any questions or comments regarding this amendment, please contact the undersigned at the number listed below.

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Respectfully submitted,  
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